Ch. 11: Practical Considerations for Digital Design
Objectives

Should be able to:

- Describe the causes and effects of a race condition on synchronous flip-flop operation.
- Use manufacturers’ data sheets to determine IC operating specifications such as setup time, hold time, propagation delay, and input/output voltage and current specifications.
- Perform worst-case analysis on the time-dependent operations of flip-flops and sequential circuitry.
- Design a series RC circuit to provide an automatic power-up reset function.
- Describe the wave-shaping capability and operating characteristics of Schmitt trigger ICs.
- Describe the problems caused by switch bounce and how to eliminate its effects.
- Calculate the optimum size for a pull-up resistor.
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1. Flip-Flop Time Parameters
2. Automatic Reset
3. Schmitt Trigger Ics
4. Switch Debouncing
5. Sizing Pull-Up Resistors
6. Practical Input and Output Considerations
A race condition occurs when the data inputs (J-K or D) to a flip-flop are changing at the same time as the active clock transition.

Set-up time is the time that the data inputs to a flip-flop must be set before the active clock transition.

Hold time is the amount of time that the data inputs must maintain their level after active clock transition.

The time required for the Q output to change as a result of some input is called the propagation delay.
  - $t_{PLH}$ is the propagation delay when the Q output goes from low to high.
  - $t_{PHL}$ is the propagation delay when the Q output goes from high to low.

The propagation delay can be caused by an asynchronous input (RD or SD) or a synchronous input (Cp).
There are several other parameters that will also be listed in a manufacturer's data sheet.

1. Maximum frequency ($F_{\text{max}}$) - The maximum frequency allowed at the clock input.
2. Clock pulse width (LOW) [$t_w(L)$] - The minimum width that is allowed at the clock input during the LOW level.
3. Clock pulse width (HIGH) [$t_w(H)$] - The minimum width that is allowed at the clock input during the high level.
4. Set or Reset pulse width (LOW) [$t_w(L)$] - The minimum width of the LOW pulse at the set or reset inputs.

There are times when a delay may need to be introduced in a signal in order for a circuit to function properly.

Special delay gate ICs are available that provide exact, predefined delays.
Figure 11-3 Setup and hold parameters for a 74LS76 flip-flop.
A series RC circuit can be used to set or reset a flip-flop when power is applied.

The voltage across the capacitor will start low and charge toward the supply voltage. This means that the set or reset function will be initially active but will be removed after a short period of time.

The amount of reset time can be increased by increasing the size of the capacitor.
3. Schmitt Trigger ICs

A Schmitt trigger is a circuit used to transform slowly changing waveforms into sharply changing, jitter free output signals.

The hysteresis is the difference in switching levels between the positive-going input and negative-going input signal.

The difference in switching voltage is called the hysteresis voltage.

The transfer function is used to illustrate the relationship between the input switching voltages and the output HIGH and LOW level voltages.
Figure 11-24  Edge-sharpening, jitter-free operation of a Schmitt trigger: (a) regular inverter; (b) Schmitt inverter.
Function Transfer

![Function Transfer Graph]

- $V_{out}$
- $V_{in}$

Values:
- $V_{out} = 3.4 \text{ V}$
- $V_{out} = 0.2 \text{ V}$
- $V_{in} = 0.9 \text{ V}$
- $V_{in} = 1.7 \text{ V}$
\[
duty \text{ cycle} = \frac{\text{time HIGH}}{\text{time HIGH + time LOW}} \times 100 \text{ percent}
\]

\[
duty \text{ cycle} = \frac{1.7 - 0.4}{(1.7 - 0.4) - (2.2 - 1.7)} = \frac{1.3}{1.3 + 0.5} = 72.2 \text{ percent}
\]
4. Switch Debouncing

Any mechanical switch is going to exhibit bounce which will result in multiple pulses.

One way to debounce a single-pole, single-throw switch is to use a Schmitt trigger circuit with a resistor and capacitor on the input.

A single-pole, double-throw switch can be debounced using a cross-coupled NAND flip-flop.

Single-pole, double-throw switches can also be debounced with any type of flip-flop that has an asynchronous set and reset input.
5. Sizing Pull-Up Resistors

Pull-up resistors must be sized to maintain the proper voltage levels given the input current requirements of the circuit.

Pull-down resistors usually are required to dissipate more power.
6. Practical Input and Output Considerations

- TTL circuits require a supply voltage of 5.0V ±5%.
- A 60 Hz. clock signal can be derived from the AC line voltage because that line frequency is very accurate.
- It is best to connect LEDs to digital outputs so that a low will turn on the LED. TTL can sink more current in the low state than it can drive in the high state.
- Phototransistors are transistors that are used to detect the presence or absence of light.
Phototransistors combined with waveshaping circuits and flip-flops can be used to make an alarm circuit.

An optocoupler is an IC with an LED and a phototransistor in the same package.

Optocouplers can be used to shift or change the output voltage level of a logic circuit.

Power MOSFETs can be connected to the outputs of logic gates to increase the current drive of the output.
Unused inputs of logic gates should never be left floating but rather should be connected such that they do not affect the circuit operation.

The inputs on AND and NAND should be tied high while the inputs on OR and NOR should be tied low.
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