Logic Families and Their Characteristics
Objectives

Should be able to:

- Analyze the internal circuitry of a TTL NAND gate for both the HIGH and LOW output states.
- Determine IC input and output voltage and current ratings from the manufacturer’s data manual.
- Explain gate loading, fan-out, noise margin, and time parameters.
- Design wired-output circuits using open-collector TTL gates.
- Discuss the differences and proper use of the various subfamilies within both the TTL and CMOS lines of ICs.
- Describe the reasoning and various techniques for interfacing between the TTL, CMOS, and ECL families of ICs.
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There are 3 commonly used families of digital IC logic:
- TTL (Transistor-Transistor Logic)
- CMOS (Complementary Metal Oxide Semiconductor)
- ECL (Emitter-Coupled Logic)

Prefix (Manufacturer)
- S Signetic
- DM National Semiconductor
- SN Texas Instruments
Cont.

- **Suffix (Package Type)**
  - N Plastic Dual in Line (DIP)
  - W Ceramic Flatpack
  - D Surface Mounted SO Plastic Package

- **54XX military version, -55 to 125 C**
- **74XX commercial version, 0 to 70 C**
1. The TTL Family

- The input of a TTL logic gate is characterized by a multi-emitter transistor.
- Each emitter is one input to the logic gate. A two input gate will have two emitters and a four input gate will have four emitters.
- The output stage of most TTL logic is a totem-pole circuit.
- When at least one input to a TTL NAND gate is low, the bottom transistor of the totem-pole output (Q4) is OFF and the top transistor (Q3) is ON, making the output a logic high.
- When all inputs to a TTL NAND gate are high, the top transistor of the totem-pole output (Q3) is OFF and the bottom transistor (Q4) is ON, pulling the output low.
Figure 9–3  Equivalent circuits for a TTL NAND in the (a) HIGH;

Figure 9–3  (Continued.) (b) LOW output states ($I = convetional current flow$).
2. TTL Voltage and Current Ratings

◆ The input currents that a gate load draws:
  • \( I_{IH} \) - (Input High Current) - 74XX = 40 \( \mu \)A
  • \( I_{IL} \) - (Input Low Current) - 74XX = -1.6 mA

◆ The output currents that a driving gate can supply:
  • \( I_{OH} \) - (Output High - source current) - 74XX = -400\( \mu \)A
  • \( I_{OL} \) - (Output Low - sink current) - 74XX = 16 mA

◆ The minus sign indicates current leaving the gate.

◆ Fan-out is the number of gate inputs that can be driven by a single output of the same family.
  • Fan-out = \( IOH/I_{IH} \) and Fan-out \( IOL/I_{IL} \)
  (The smaller of these two values would be used if they are not the same value.)
9. Logic Families & Characteristics
Cont.

- The actual output current from a gate would be the number of gate inputs connected to the circuit multiplied by the input current of each gate.

- The voltage on the output of a TTL gate:
  - \( V_{OH} \) (output high) - 74XX = 2.4 V(min), 3.4 V(typ)
  - \( V_{OL} \) (output low) - 74XX = 0.2 V(typ), 0.4 V(max)

- The required limit of the input voltage in order to guarantee operation:
  - \( V_{IH} \) (input high) -- 74XX = 2.0 V(min)
  - \( V_{IL} \) (input low) - 74XX = 0.8 V(max)

- The noise margin is the difference between the guaranteed output voltage level and the required input voltage level of a logic gate.
  - low level noise margin = \( V_{IL} - V_{OL} = 0.4 \) V(74XX)
  - high level noise margin - \( V_{OH} - V_{IH} = 0.4 \) V(74XX)
3. Other TTL Considerations

- For a non-ideal waveform the rise time is a measure of the time required for the leading edge of the waveform to rise from 10% to 90% of its nominal amplitude.
- For a non-ideal waveform the fall time is a measure of the time required for the trailing edge of the waveform to fall from 90% to 10% of its nominal amplitude.
- The propagation delay is a measure of the time it takes the output of a logic gate to respond to a change on the input. The propagation delay is caused by the circuit of the logic gate.
  - $t_{PLH}$ is the propagation delay as the output waveform moves from low-to-high.
  - $t_{PHL}$ is the propagation delay as the output waveform moves from high-to-low.
The current drawn from the power supply by an IC is called ICC. This is usually given as two values:
- ICCH is supply current when all outputs are high.
- ICCL is supply current when all outputs are low.

The average supply current is the sum of ICCH and ICCL divided by two.

The power dissipation (PD) of an IC is the supply voltage Vcc multiplied by the average supply current Icc(avg).

When the upper transistor of a TTL totem-pole output is removed, the circuit is called an open collector output.

Any open collector output requires an external pull-up resistor for the high level current path.

Special open collector circuits called buffer/drivers are available for applications requiring large sink currents.

The open collector circuit is used whenever two or more outputs of logic gates are to be connected together.
The connecting together of two or more outputs forms a logical AND function and is called a wired-AND logic.

Many of the standard TTL logic gates are also available in open collector arrangements.

Unused inputs on AND and NAND gates should be connected high while unused inputs on OR and NOR gates should be tied low.

Any unused gate on a chip should have the inputs connected so that its output is high. (AND and OR gate inputs high; NAND and NOR gate inputs low.)

Decoupling capacitors (.01 uF to 0.1 uF) should be used on all TTL IC's between the Vcc and GND pin.

The capacitors help to reduce TTL switching noise.
4. Improved TTL Series

- Schottky TTL (74SXX) uses schottky-clamped transistors to reduce the propagation delay by 4 and increase the power consumption by only 2.
- Low-power schottky (74LSXX) has reduced power consumption from the schottky TTL.
- Advanced low-power schottky (74ALSXX) has further reductions in propagation delay and power consumption.
- Fast TTL (74FXX) has reduced propagation delay from the LS and ALS series.
5. The CMOS Family

- The CMOS family uses a complementary pair (one N-channel and one P-channel) of MOSFET devices.
- The CMOS family has a high input impedance and a very low power consumption.
- If the input to a CMOS gate is high, the N-channel device will be ON pulling the output to Ground.
- If the input to a CMOS gate is low, the P-channel device will be ON raising the output to VDD.
- CMOS logic is available in either NAND or NOR configurations.
- CMOS devices must be handled very carefully to avoid damage from static discharge.
- CMOS chips are available in almost all the same logic configurations as TTL as well as several that are unique to CMOS.
There are several families of CMOS logic:

- 4000 series - the original series.
- 40H00 series - faster.
- 74C00 series - pin compatible to TTL
- 74HC00 series - high speed pin compatible to TTL
- 74HCT00 series - input/output voltage compatible to TTL

The latest series of logic to come out is the BiCMOS series which combines the best features from both the bipolar transistors and CMOS transistors.

These BiCMOS combine high speed switching with very low power consumption. They also have a very low power consumption when idle (or inactive).

The BiCMOS logic is usually limited to microprocessor bus interface logic.
6. Emitter-Coupled Logic

- ECL logic is very fast but has an increased power consumption.
- ECL uses a differential amplifier as its basic circuit.
- ECL is very fast because the transistors are not allowed to saturate.
- The voltage levels for ECL (-0.8 V and -1.7 V) are unusual and not compatible to TTL or CMOS logic.
- The ECL logic gates usually have both an OR and a NOR output.
- New technologies are continually being developed in an effort to improve the logic.
7. Comparing Logic Families

- Major parameters for comparing logic families are the propagation delay, the power dissipation and the speed-power product.
- The power dissipation of CMOS logic depends heavily upon the operating frequency of the logic.
8. Interfacing Logic Families

- When using TTL logic to drive CMOS logic the high level voltage of the TTL output must be increased with a pull-up resistor.
- When CMOS logic is expected to drive TTL logic, the CMOS gate may not have the current capability to drive the TTL gate. In this case, special buffer drivers (4050B) gates can be used.
- Any time one logic family is connected to another logic family, the input and output voltage and current requirements for each family should be reviewed to determine the interface needs for the circuit connection.
- When the two logic families being interfaced have different power supplies then special circuits called level shifters or translators must be used.
Level Shifting
ECL Interfacing
9. Additional Notes

- The tri-state buffer is a standard TTL logic gate to which has been added an additional enable input.
- This enable input, when enabled, allows the buffer to react as a standard TTL inverter.
- When the enable input is disabled, however, the buffer has a third condition on the output. This is called the high-impedance state (high-Z) and is characterized by no current (sink or source) in the output lead. The enable input (when not active) will allow both transistors of the totem-pole output to be turned OFF.
- This means that no current can flow in the output circuit and it is as if the output pin is disconnected from the circuit.
The tri-state buffer is useful when interfacing TTL logic to a common connection (wired-AND).

If the open collector gate is used for the common connection, the overall speed is reduced because the open collector circuit has a larger propagation delay than standard TTL.

The tri-state buffer, on the other hand, retains the same propagation delay as the rest of its family.

Therefore, the tri-state buffer operates faster than the open collector circuit. In order to use the tri-state buffer, however, it must be guaranteed that only one buffer will be enabled at a time.
Totem Pole Output: